IN THE CLAIMS

1. (Currently amended) In a processing system having a processor coupled to a system bus, a method of operating a device, comprising:

instructing the processor to operate with the device;

putting information on the system bus;

retrieving the information with a memory map controller interface;

accessing a template of the device with the memory map controller interface responsive to the information;

putting device information onto an external interface bus according to the information and the template; and

operating the device according to the device information, wherein the information comprises a mode of operation, chip select, access type, and an address.

2. (Original) The method of claim 1, wherein the device is an LCD controller, co-processor, peripheral device, graphic accelerator, imaging device or simply any peripheral with addressable registers or memory.

3. (Original) The method of claim 1, wherein the system bus contains an address bus.

4. (Original) The method of claim 1, wherein the information comprises a method of operation of the device.

5. (Original) The method of claim 4, wherein the method of operation is selected from a group consisting of read and write.

6. (Canceled).

7. (Original) The method of claim 1, wherein the template is selected from a plurality of templates stored in a memory coupled to the system bus, further wherein at least one template is optional on a per access/device type basis.

8-11. (Canceled).

12. (Currently amended) A processing system for controlling devices via an external interface bus comprising:

a processor coupled to a system bus;

a memory coupled to the system bus for storing templates for describing operating characteristics of the devices; and

a memory map controller interface coupled to the system bus and to an external interface bus, wherein the memory map controller interface is further characterized as receiving information from the processor via the system bus and receiving templates from the memory via the system bus, and wherein the received information comprises a mode of operation, chip select, access type, and an address.

13.-14. (Canceled)

15. (Currently amended) The processing system of claim [[14]] 12, wherein the templates comprise data about operating characteristics of the devices.

16. (Currently amended) The processing system of claim [[13]] 12, wherein the templates comprise access protocols of the devices.

17. (Currently amended) The processing system of claim [[13]] 12, wherein at least one of the templates is for a display controller.

18. (Currently amended) The processing system of claim [[13]] 12, wherein the system bus comprises an address bus.

19. (Currently amended) A processing system, comprising:

a processor coupled to a system bus;

a memory coupled to the system bus for storing a plurality of templates; and

a controller ~~means,~~ coupled to the system bus and to an external interface bus, ~~for responding to information provided by the processor concerning a device by~~

~~retrieving~~ wherein the controller is configured to retrieve a template of the plurality of templates in response to information received from the processor via the system bus and ~~providing~~ further configured to provide the information, in a manner consistent with the retrieved template, on the external interface bus, wherein the information comprises a mode of operation, chip select, access type, and an address.

20. (Original) The processing system of claim 19, wherein each template corresponds to a type of device and a mode of operation for the type of device.

21. (Currently amended) The processing system of claim 20, wherein the memory ~~the~~ stores an operating system that identifies devices that are to be accessed.

22. (Original) The processing system of claim 21, wherein the information provided by the processor to the controller means specifies a mode of operation.

23. (Original) The processing system of claim 22, wherein at least one of the plurality of templates is for a display controller.

24. (Canceled).

25. (Original) The processing system of claim 19, wherein the templates comprise access protocols of the devices.